PVP 14

Code: EE2T4

I B.Tech - II Semester - Regular / Supplementary Examinations – May 2017

BASIC ELECTRONIC DEVICES AND CIRCUITS
(ELECTRICAL & ELECTRONICS ENGINEERING)

Duration: 3 hours Max. Marks: 70

PART – A

Answer ***all*** the questions. All questions carry equal marks

11x 2 = 22 M

1.

a) Name the diode that works as a Voltage Variable Capacitor and briefly explain its principle of operation.
b) A Full wave Rectifier delivers 50W to a load of 200Ω. If the ripple factor is 1%, calculate the ac ripple voltage across the load.
c) Establish the relation between Transconductance g_m, Drain resistance r_d and amplification factor μ of a FET.
d) Can you make distinction between MOSFET and FET.
e) An amplifier has an open loop gain of 90. When a negative feedback of feedback factor 0.6 is applied to it, calculate the overall gain.
f) Why do you think RC Oscillators are more suitable for low frequency applications? How would you categorize RC oscillators?

g) How would you prove that the BJT is biased in its linear or active operating region?

h) Why do you think Bias Stabilization is required in transistors? Explain briefly.

i) Briefly explain the principle of operation of LC Tank circuit.

j) Derive the gain with Feedback for a Voltage-Shunt Feedback network.

k) Obtain the relationship between α and β of a BJT.

PART – B

Answer any ***THREE*** questions. All questions carry equal marks.

3 x 16 = 48 M

2. a) Describe how diffusion and Transition Capacitances differ? 8 M

b) A FWR circuit is fed from a transformer having a center tapped secondary winding. The rms voltage from either end of secondary to center tap is 30V. If the diode forward resistance is 2Ω and that of the half secondary is 8Ω, for a load of 1KΩ calculate,

(i) Power delivered to the load

(ii) Efficiency of rectification

(iii) TUF of secondary 8 M

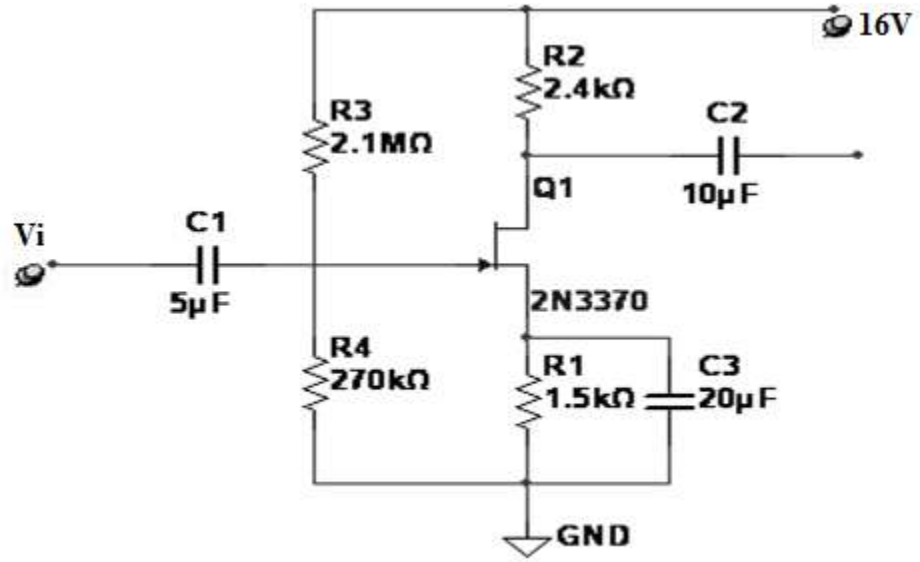
3. a) Describe the operation of n-channel JFET and justify that it is a voltage controlled device. 8 M

b) Define Early Effect. Draw and explain the BJT configuration in which you come across this effect. 8 M

4. a) Design a Voltage divider bias circuit for the specified conditions. V_{cc}=12V, V_{CE} = 6V, I_c =1 mA, S=20, β=100 and V_E =1V. 8 M

b) Determine the following for the network shown.

i) I_{DQ} ii) V_D iii) V_{DS}



I_{DSS} =8mA, V_p =-4V , V_{DD}=16V. 8 M

5. a) Draw the circuit diagram of CE amplifier with emitter resistance and obtain its equivalent hybrid model. Also derive expressions for A_I, R_I. 8 M

b) Why do you think hybrid model is not suitable for high frequency analysis of BJT? Draw hybrid-π model and obtain the basic parameters. 8 M

6. a) Determine the voltage gain, input & output impedance with feedback for Voltage series having A=-100, R_i =10K & R_o =20K for a feedback of i) β=-0.1 & ii) β=-0.5. 8 M

b) Explain the operation of RC - Phase shift oscillator with the help of neat circuit diagram. 8 M